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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/385,394	08/30/1999	JOHN S. YATES JR.	30585/3	9093

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EXAMINER	
ELLIS, RICHARD L	
ART UNIT	PAPER NUMBER
2183	11

DATE MAILED: 10/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/385,394	Yates Jr. et al.
Examiner	**Group Art Unit**
Richard Ellis	2183

--The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address--

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE 3 (Three) MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) Months from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on June 26, 2002.

☒ This action is FINAL

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-133. is/are pending in the application.

☐ Of the above claim(s) _____ is/are withdrawn from consideration.

☒ Claim(s) 1-21 and 37-50. is/are allowed.

☒ Claim(s) 22-28, 30-33, 51-59, and 61-133. is/are rejected.

☒ Claim(s) 34-36 and 60. is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119(a)-(d)

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of References Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent drawing Review, PTO-948

☐ Other _____

Office Action Summary

1. Claims 1-95 remain for examination. Claims 96-133 are newly presented for examination.

2. Applicant's indication that format drawings were filed November 14, 2000 is acknowledged. However, the PTO file does not contain any formal drawing prints. The filed formal drawings are likely lost, and applicant should resubmit the formal drawings in order to complete the file.

3. New claims 97-100 and 102-103 are rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A) The following terms lack proper antecedent basis:

1. "the first calling convention", "the second calling convention" claim 97;
2. "the two conventions are two calling conventions" claim 98;
3. "the two calling conventions", "the other calling convention" claim 99;
4. "the first calling convention", "the second calling convention" claim 100;
5. "the first calling convention", "the second" claim 102;
6. "the first calling convention", "the second" claim 103.

4. The text of those sections of Title 35, US Code not included in this action can be found in a prior Office Action.

5. Claims 51-59, 61-75, 77-78, and 94 are rejected under 35 USC 102(b) as being clearly anticipated by Richter et al., U.S. Patent 5,481,684.

6. Claims 22-33, 76, 79-85, 87-93, and 95 are rejected under 35 USC § 103 as being unpatentable over Richter et al., U.S. patent 5,481,684.

Richter et al. was cited as a prior art reference in paper number 8, mailed Feburary 20, 2002.

7. The rejections are respectfully maintained and incorporated by reference as set forth in the last office action, paper number 8, mailed Feburary 20, 2002.

8. Applicant's arguments filed June 26, 2002, paper number 10, have been fully considered but they are not deemed to be persuasive.

9. As to newly broadened claim 22 (see pg. 24, section V. of the response), it does not teach or define above the invention claimed in previous claim 3 and is therefore rejected under Richter et al. for the same reasons set fourth in the previous rejection of claim 3.

10. New claims 96-98, 102-111, 113-115, and 128-133 are rejected under 35 USC 102(b) as being clearly anticipated by Richter et al., U.S. Patent 5,481,684.

11. As to claim 96, Richter et al. taught a microprocessor chip, comprising:

A) two instruction decoders (fig. 5, "CISC ID", "RISC ID" designed to decode instructions of first and second instruction sets (CISC & RISC), respectively, and circuitry of a single instruction pipeline (48) designed to execute the instructions decoded by either of the two instruction decoders;

B) circuitry and/or software (42) designed to detect when execution flows or transfers control from code coded in one instruction set to code coded in the other (col. 10 lines 30-45), program code in the first and second instruction sets using first and second different data storage conventions (col. 9 lines 17-26), respectively; and,

C) circuitry and/or software designed to respond to the detection by altering the data storage content of the computer to create a program context under the second data storage convention that is logically equivalent to a pre-alteration program context under the first data storage convention (col. 9 lines 17-26).

12. As to claim 97, Richter et al. taught that the memory unit and software are designed to effect a transition between instruction boundaries (col. 3 line 40 to col. 6 line 39), between execution in a region coded in the first instruction (CISC) set using the first calling convention (CISC) to execution in a region coded in the second instruction set (RISC) using the second calling convention (RISC), so that code at the source of the flow or transfer may effect the execution transition without being specially coded for code at the destination (col. 6 lines 27-39).

13. As to claim 98, Richter et al. taught two calling conventions, RISC and CISC conventions.

14. As to claim 102, Richter et al. taught that a rule for altering the data storage content

from the first calling convention to the second is determined based on an instruction at the location of execution at the source of the recognized execution flow or transfer (col. 9 lines 26-57).

15. As to claim 103, Richter et al. taught a rule for altering the data storage content from the first calling convention to the second was determined by examining a descriptor associated with the location of execution before the recognized execution flow or transfer (col. 9 lines 17-57).

16. As to claim 104, Richter et al. taught executing instructions fetched from first and second regions of a single address space (col. 2 lines 20-36), the instructions of the first and second regions being coded for execution by computers of first and second architectures (RISC & CISC) or following first and second data storage conventions (col. 9 lines 17-26), respectively , the memory regions having associated first and second modifiable indicator elements (fig. 4), a hardware structure for storing the indicator elements enforcing a requirement that the memory regions be necessarily disjoint (col. 7 line 27 to col. 8 line 25), the modifiable indicator elements each having a value indicating the architecture or data storage convention under which instructions from the associated region are to be executed (col. 9 lines 10-17);

when execution of the instruction data flows or transfers from the first region to the second, adapting the computer for execution in the second architecture or convention (col. 9 lines 27-57 and col. 10 lines 30-46).

17. As to claim 105, Richter et al. taught the regions are pages managed by a virtual memory manager (col. 6 lines 45-50 and col. 7 lines 26-44).

18. As to claim 106, Richter et al. taught the modifiable indicator elements are stored in a table, each modifiable indicator element associated with a corresponding physical page frame (col. 9 line 59).

19. As to claim 107, Richter et al. taught that the entries are entries of a translation look-aside buffer (col. 7 lines 11-26).

20. As to claim 108, Richter et al. taught that the two architectures were two instruction set

architectures (CISC & RISC), and wherein the adapting step included controlling instruction execution hardware of the computer to interpret the instructions according to the two instruction set architectures according to the modifiable indicator elements (col. 9 lines 27-57 and col. 10 lines 30-45).

21. As to claim 109, Richter et al. taught that one of the regions stores an off-the-shelf operating system binary coded in an instruction set non-native to the computer, the non-native instruction set providing access to a reduced subset of the resources of the computer (col. 3 lines 16-40 and col. 9 lines 42-57).

22. As to claims 110-111, Richter et al. taught that the two conventions were first and second data storage conventions (col. 9 lines 17-27), and recognizing when program execution has flowed or transferred from a regions whose modifiable indicator element indicates the first data storage convention to a region whose modifiable indicator element indicates the second data storage convention, and in response to the recognition, altering the data storage content of the computer to create a program context under the second data storage convention that is logically equivalent o a pre-alternation program context under the first data storage convention (col. 9 lines 17-57 and col. 10 lines 30-45).

23. As to claims 113-115, 128-133, they do not teach or define above the invention claimed in claim 96-98, 102-111, and 113-115 and are therefore rejected under Richter et al. for the same reasons set fourth in the rejection of claim 96-98, 102-111, and 113-115, supra.

24. As to claim 133, Richter et al. taught raising an exception when execution flowed or transferred from a region whose indicator element indicated one architecture or execution convention to another (col. 3 lines 9-15).

25. New claims 99-101, 112, 116-127 are rejected under 35 USC § 103 as being unpatentable over Richter et al., U.S. patent 5,481,684, as applied to claims 96-98, 102-111, 113-115, and 128-133, supra.

26. As to claim 99, Richter et al. did not specifically teach that one calling convention was register-based, and the other was memory stack based. However, as is notoriously well known in the prior art, RISC calling convention is traditionally a register-based calling convention due

to the larger number of registers in a RISC chip, and CISC calling convention is traditionally a memory stack based calling convention due to the smaller number of registers in a typical CISC chip. Accordingly, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to have implemented calling convention conversion between register-based and memory stack based conventions because doing so is required to produce a processor that is properly capable of performing as described by Richter et al., e.g., with one architecture (CISC) transparently calling another architecture (RISC) (col. 6 lines 23-39 and col. 9 lines 17-27).

27. As to claim 100, Richter et al. did not teach specifically software and/or hardware designed to copy a datum from a first location to a second location, the first location having a use under the first calling convention analogous to the use of the second location under the second calling convention. However, it would have been immediately inherently evident to one of skill in the art that it was inherently required to copy a datum from one location to another location (e.g., stack to register or register to stack) in order to convert between two calling conventions, register-based and stack based. This is required because to do otherwise does not convert between the two conventions, which would result in a system that does not provide Richter et al. transparent calling of RISC routines by CISC code, and CISC routines by RISC code.

28. As to claim 101, Richter et al. taught that it was necessary to convert between data storage conventions, and it is inherent that to do so one must copy data from a location under the first data storage convention to another equivalent location under the second data storage convention (col. 9 lines 17-27). It is also inherently evident that once copied, the source location is no longer required by the execution of the program using the new data storage convention.

29. As to claim 112, Richter et al. did not specifically teach that one calling convention was register-based, and the other was memory stack based. However, as is notoriously well known in the prior art, RISC calling convention is traditionally a register-based calling convention due to the larger number of registers in a RISC chip, and CISC calling convention is traditionally a

memory stack based calling convention due to the smaller number of registers in a typical CISC chip. Accordingly, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to have implemented calling convention conversion between register-based and memory stack based conventions because doing so is required to produce a processor that is properly capable of performing as described by Richter et al., e.g., with one architecture (CISC) transparently calling another architecture (RISC) (col. 6 lines 23-39 and col. 9 lines 17-27).

30. As to claims 116-127, they do not teach or define above the invention claimed in claims 99-101 and 112 and are therefore rejected under Richter et al. for the same reasons set fourth in the rejection of claims 99-101, 112, supra.

31. In the remarks, applicant argues in substance:

A) That: "Richter '684 teaches nothing analogous to 'altering the data storage content of the computer' in the manner recited in claim 22."

This is not found persuasive because Richter et al. clearly teaches that the data storage content of the computer must be altered "when program execution has flowed or transferred from a region whose indicator element indicates the first data storage contention to a region whose indictor [sic] element indicates the second data storage convention" at col. 9 lines 17-26).

B) That: "Richter's 'segment descriptors' and 'segment registers' are associated with segments. See, *e.g.*, Richter '684 at col. 6, line 40 to col. 8, line 25. In contrast, claim 51 recites that the indicator elements are associated with 'pages.'"

This is not found persuasive because to the extent defined by the exact meaning of the claim language, the reference to "pages" is merely an indication that there are sections or portions of memory managed by a memory manager. Because segments are also sections or portions of memory managed by a memory manager, they meet the limitation recited in the claim language.

C) That: As to claim 87 "The Office Action characterizes Richter '684 as indicating 'the necessity of transforming aspects specific to one architecture into the appropriate aspect specific to the other architecture.' ... Richter '684 fails to teach any technique for actually performing that 'transforming.' (emphasis unchanged)

This is not found persuasive because it should be pointed out that applicant's claims fail to claim any technique for actually performing that 'transforming.' Applicant's claims only claim that such a transformation occurs, but do not claim any specific technique. Absent claim language detailing a specific technique for performing the transformation, applicant's claims can not be read over Richter et al.'s indication that the transformation also must occur.

D) That: "The one portion of a solution discussed by Richter '684, the switch from big-endian to little-endian, col. 9, lines 17-26, does not involve "at least one data movement operation" as recited in claim 87.

This is not found persuasive because it would be immediately apparent that in order to perform Richter et al.'s stated goal of allowing access to RISC data structures from CISC code, or CISC data structures from RISC code will inherently involve "at least one data movement operation" because there is no other way to convert from RISC data structures to CISC data structures without movement of data in some manner.

E) That: As to claims 94 and 96 "Richter '684, at col. 13 line 48 to col. 14 line 5, teaches only that the hardware has some capability to execute two different instruction sets. This section teaches nothing to indicate that a transferor in one instruction set can simply transfer control to a transferee, oblivious of what the transferee routine might be, without carefully preparing to transfer to the transferee in the correct way."

This is not found persuasive because applicant's argument is directed to the entire purpose for the whole Richter et al. disclosure, namely that of seamlessly and invisibly transferring control from one instruction set to another, without the necessity of any careful setup on the part of either routine. See for example col. 6 lines 27-39, col. 9 lines 26-57, and col. 14 lines 33-43.

F) That: As to claims 104 and 113 "The claim recites that the computer hardware requires that 'the memory regions be necessarily disjoint.' ... As is well known in the art, Intel segments may - and frequently do - overlap. For example, it is fairly common for Intel programs to run with the code, data, and stack segments exactly overlaying each other."

This is not found persuasive because by applicant's own admission, Intel segments only "**may**" overlap. They are not required to overlap and therefore, in those situations where they do not overlap, they do properly anticipate the claim language.

32. Claims 1-21 and 37-50 are allowable over the prior art of record.

33. Claim 34-36 and 60 are objected to as being dependent upon a rejected base claim, but would render the base claim allowable if bodily incorporated into the base claim such that the new base claim included all of the original limitations of the base claim, any intervening claims, and the objected claim.

34. Applicant's amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 CFR § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

35. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (703) 305-9690. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (703) 305-9712. The fax phone numbers for this Group are: After-final: (703) 746-7238; Official: (703) 746-7239; Non-Official/Draft: (703) 746-7240.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Richard Ellis
September 30, 2002

Richard Ellis
Primary Examiner
Art Unit 2183